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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,244	07/03/2003	Hung-En Tai	LKSP0017USA	1243

27765 7590 09/10/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
LE, TOAN M	
ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,244	TAI ET AL.	
	Examiner	Art Unit	
	Toan M Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

It does not identify the foreign application for patent or inventor's certificate on which priority is claimed pursuant to 37 CFR 1.55, and any foreign application having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month and year of its filing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by "Data Mining and Fault Diagnosis Based on Wafer Acceptance Test Data and In-line Manufacturing Data", Fan et al. (referred hereafter Fan et al.).

Referring to claim 1, Fan et al. disclose a method for analyzing in-line quality control (QC) test parameters (Abstract), the method being used to analyzed a plurality of lots of products, each lot of products comprising a lot number, the products being formed using a plurality of equipments, at least one wafer of each lot of products being tested by at least one in-line QC test item to generate an in-line QC test parameter, the in-line QC test item, and its sample test item and wafer test item being stored in a database, the database further storing the in-line QC test parameter and data of a plurality of lots of high-yield product stocks, such as test

items and test parameters (page 172, 2nd col., Control Policy Re-evaluation section: lines 1-18; figure 1), the method comprising:

analyzing the in-line QC test parameter to determine whether the in-line QC test parameter corresponds to a predetermined spec or not (page 172, 2nd col., Fab Data Case Study section: lines 1-6);

searching the database to find out the sample test item or the wafer test item related to the in-line QC test item when the in-line QC test parameter does not correspond to the predetermined spec;

searching the database to find out the corresponding test parameters of the high-yield product stocks according to the in-line QC test item and the searched sample test item or the wafer test item (page 172, 2nd col., Fab Data Case Study section: lines 7-15; figure 3); and

generating a correlation to illustrate the relationship between the in-line QC test item and the sample test item, or the relationship between the in-line QC test item and the wafer test item according to the searched high-yield product stocks (page 172, 2nd col., Fab Data Case Study section: lines 16-18; page 173, 1st col., lines 8-24).

As to claim 2, Fan et al. disclose the method as described above wherein the lots of products are not tested by a sample test process and a wafer test process (page 172, 2nd col., Fab data Case Study section: lines 16-18; figure 4).

Referring to claim 3, Fan et al. disclose the method as described above wherein the correlation between the in-line QC test item and the sample test item, and the correlation between the in-line QC test item and the wafer test item are generated using linear regression methods (page 172, 1st col., 2nd half; and 2nd col., Fab Data Case Study section: lines 16-18).

As to claim 4, Fan et al. disclose the method as described above further comprising: predicting the sample test result of the lots of products according to the in-line QC test parameter not corresponding to the predetermined spec, and according to the correlation between the in-line QC test item and the sample test item (page 172, 1st col., 2nd half; page 172, 2nd col., lines 1-7 and Fab Case Study section: lines 16-18; figure 4).

Referring to claim 5, Fan et al. disclose the method as described above further comprising: predicting the wafer test result of the lots of products according to the in-line QC test parameter not corresponding to the predetermined spec, and according to the correlation between the in-line QC test item and the wafer test item (page 172, 1st col., 2nd half; page 172, 2nd col., lines 1-7 and Fab Case Study section: lines 16-18; figure 4).

As to claim 6, Fan et al. disclose the method as described above wherein the database stores data of a process step related to the in-line QC test item, and the method further comprises:

classifying the lots of products into two groups according to a first spec, the two groups of products comprising a qualified group of products corresponding to the first spec, and a failed group of products not corresponding to the first spec (page 172, 1st col., Device variatuin Partition section: lines 1-5);

searching the database to find out the process step related to the in-line QC test item;

finding the equipments used in the process step according to the lot numbers of the two groups of products; and

determining the equipment through which a probability that the failed group of products have passed is higher than a probability that the qualified group of products have passed (page 172, 1st col., Key Node Screening section: lines 1-5).

Referring to claim 7, Fan et al. disclose the method as described above wherein commonality analysis is used to determine the equipment through which a probability that a low-yield group of products have passed is higher than a probability that a high-yield group of products have passed (page 172, 1st col., Key Node Screening section: lines 1-5 and 2nd col., Fab Data case Study section: lines 7-15) .

As to claim 8, Fan et al. disclose the method as described above further comprising: searching test results of each of the sample test items and each of the in-line QC test items of the lots of products after a sample test process of the lots of products; and generating a correlation between each of the sample test items and each of the in-line QC test items according to the search results (page 172, 2nd col., Control Policy re-evaluation section: lines 1-18).

Referring to claim 9, Fan et al. disclose the method as described above wherein the correlation between each of the sample test items and each of the in-line QC test items is generated by a multiple regression model (page 171, 2nd col., 2nd paragraph).

As to claim 10, Fan et al. disclose the method as described above wherein the correlation between each of the sample test item and each of the in-line QC test items is generated by a stepwise regression model (page 171, 2nd col., 2nd paragraph).

Referring to claim 11, Fan et al. disclose the method as described above wherein the correlation between each of the sample test items and each of the in-line QC test items is illustrated by a residual plot (page 172, 1st col., 2nd half, equation 1, "e_i is a modeling residual").

As to claim 12, Fan et al. disclose the method as described above further comprising:

searching test results of each of the sample test items and each of the in-line QC test items of the lots of products after a sample test process of the lots of products;

classifying the lots of products into a plurality of groups according to the parameters of each of the in-line QC test items of the lots of products (page 172, 1st col., Device Variation Partition section: lines 1-5; figure 3);

analyzing the sample test parameters of each group of products (page 172, 2nd col., Fab Data Case Study section: lines 1-6); and

analyzing and obtaining the group of products having the sample test parameters most similar to a second spec when the sample test parameters of the groups of products are different (page 172, 2nd col., Fab Data Case Study section: lines 7-15).

Referring to claim 13, Fan et al. disclose the method as described above wherein an ANOVA method is used to analyze whether the sample test parameters of the groups of products are different or not (page 171, 2nd col., 2 paragraph).

As to claim 14, Fan et al. disclose the method as described above wherein a Duncans multiple range test is used to analyze and obtain the group of products having the sample test parameters most similar to the predetermined spec (figures 7-9).

Referring to claim 15, Fan et al. disclose the method as described above wherein the classified lots of products are illustrated by a box plot (figure 3).

As to claim 16, Fan et al. disclose the method as described above wherein each of the in-line QC test parameters of the obtained group of products is used as a predetermined spec of the subsequent products (figure 1).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,761,064 to La et al. U.S. Patent No. 6,708,073 to Heavlin

U.S. Patent No. 6,477,432 to Chen et al.

"In-line Statistical Process Control and Feedback for VLSI Integrated Circuit Manufacturing", Scher et al., IEEE 1989, Pages 70-75.

"In-line Defect sampling Methodology in Yield Management: An Integrated Framework", Nurani et al., IEEE Transactions on Semiconductor Manufacturing, November 1996, Vol. 9, No. 4, Pages 506-517.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

September 1, 2004

John Barlow
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